PHYS325 - Electromagnetism
Experiment 2 - Digital Logic Circuits

Glenn Harris
2117277

February 28, 2005

Introduction

Some stuff about logic and circuit design goes here

Results

Part 4

A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

Table 1: Truth table for A XOR B.

Using Table 1, the expression for the *exclusive or* function is $\overline{A}.B + A.\overline{B}$.

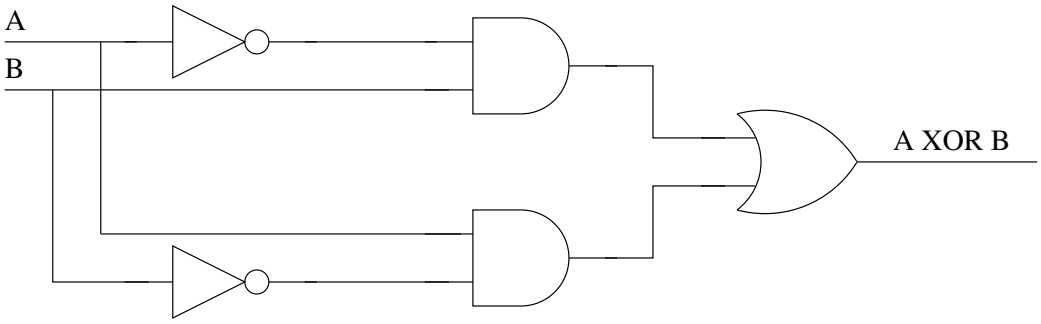

Figure 1: Exclusive Or circuit

Part 5

Using the results from the Table 2 below, the expressions for S and C are:

$$\begin{aligned} S &= \overline{A}.B + A.\overline{B} \\ &= A \oplus B \\ C &= A.B \end{aligned}$$

The expressions for S and C_{out} are:

$$\begin{aligned} S &= \overline{A}.\overline{B}.C_{in} + \overline{A}.B.\overline{C_{in}} + A.\overline{B}.\overline{C_{in}} + A.B.C_{in} \\ C_{out} &= \overline{A}.B.C_{in} + A.\overline{B}.C_{in} + A.B.\overline{C_{in}} + A.B.C_{in} \end{aligned}$$

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 2: Truth table for the Half Adder.

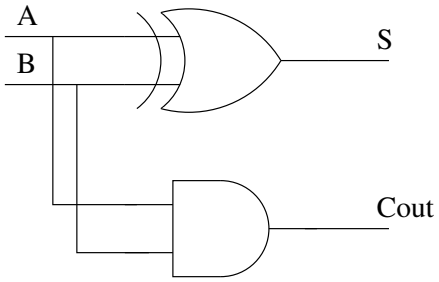

Figure 2: Half Adder Circuit

A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 3: Truth table for the Full Adder.

The expressions derived for S and C_{out} from Table 3 can be simplified, using DeMorgan's Theorem and Boolean identities, as shown below.

$$
\begin{aligned}
S &= A.\overline{B}.\overline{C_{in}} + \overline{A}.B.\overline{C_{in}} + \overline{A}.\overline{B}.C_{in} + A.B.C_{in} \\
&= A.\overline{B}.\overline{C_{in}} + \overline{A}.B.\overline{C_{in}} + (\overline{A}.\overline{B} + A.B)C_{in} \\
&= A.\overline{B}.\overline{C_{in}} + \overline{A}.B.\overline{C_{in}} + (A.\overline{A} + \overline{A}.\overline{B} + A.B + B.\overline{B})C_{in} \\
&= A.\overline{B}.\overline{C_{in}} + \overline{A}.B.\overline{C_{in}} + ((\overline{A} + B).(A + \overline{B}))C_{in} \\
&= A.\overline{B}.\overline{C_{in}} + \overline{A}.B.\overline{C_{in}} + \overline{(A.\overline{B}.\overline{A}.B)}C_{in} \\
&= (A.\overline{B} + \overline{A}.B)\overline{C_{in}} + (A.\overline{B} + \overline{A}.B)C_{in} \\
&= (A.\overline{B} + \overline{A}.B) \oplus C_{in} \\
&= (A \oplus B) \oplus C_{in}
\end{aligned}
$$

$$
\begin{aligned}
C_{out} &= \overline{A}.B.C_{in} + A.\overline{B}.C_{in} + A.B.\overline{C_{in}} + A.B.C_{in} \\
&= (A.\overline{B} + \overline{A}.B)C_{in} + AB(C_{in} + \overline{C_{in}}) \\
&= (A \oplus B)C_{in} + A.B
\end{aligned}
$$

By comparing the above expressions with those obtained for the half adder circuit in FIgure 2 with those above, it can be seen that a full adder circuit can be constructed by using two half adder circuits combined with an *OR* gate. The circuit diagram for the full adder circuit is shown in FIgure 3 below.

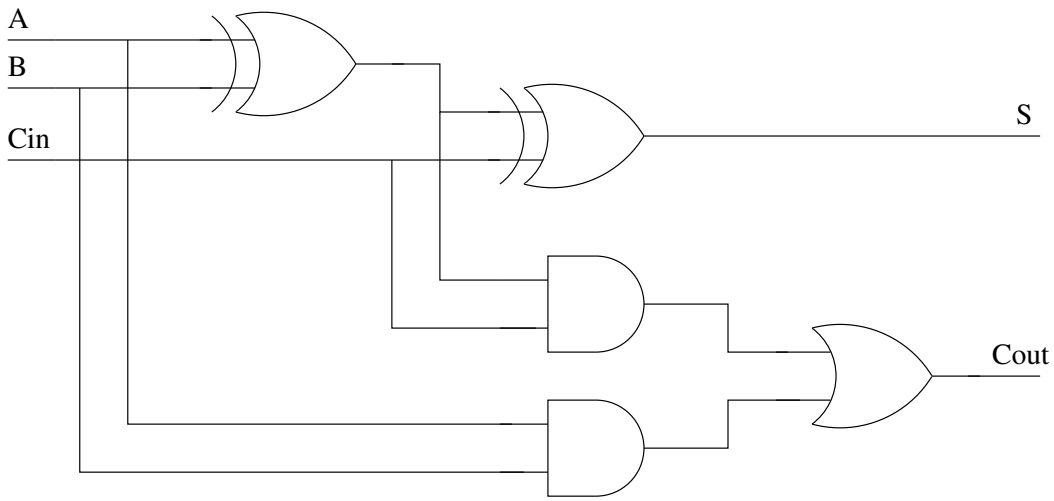

Figure 3: Full Adder Circuit